REMARKS

Claim 27 is pending in the above-identified application.

In the Office Action of May 2, 2007, claim 27 was rejected as anticipated by Akimoto et al. (US4942474)..

In response to the rejection, claim 27 has been amended to clarify that the horizontal scanning circuit is not part of the reset element. Further, the various interconnections among the recited elements have been clarified.

The background of the operation of *Akimoto et al.* is described in the paragraph bridging Columns 2 and 3 in connection with Figure 3:

> An example of the above solid-state imaging device will be explained below, with reference to FIG. 3. FIG. 3 is a circuit diagram showing this example. Referring to FIG. 3, photoelectric conversion elements (for example, photodiodes) 1 store electric charges corresponding to incident light, and are arranged so as to form a two-dimensional matrix. A photodiode 1 is connected to a reset switch 3 and the gate of a pixel amplifier 4 through a vertical gate switch 2 which is controlled by a vertical gate line 5, and a horizontal gate switch 43 which is controlled by a horizontal gate line 51. The drain electrode of the pixel amplifier 4 is connected to a drain line 44, and the source electrode of the pixel amplifier 4 is connected to a load transistor 49 through a horizontal signal line 45, a read-out gate switch 47 and a vertical signal line 48. The circuit elements 4, 45, 47, 48 and 49 make up a source follower circuit. Now, explanation will be made of the operation of a single pixel which is selected by a horizontal scanning circuit (for example, horizontal register) 22 and a vertical scanning circuit (for example, vertical

register) 21. A reset operation is first performed by the reset switch 3, and the source follower circuit including the pixel amplifier 4 is operated to deliver an output signal which is obtained in a reset period, from an output terminal 50. Next, the signal charge stored in the photodiode 1 is supplied to the pixel amplifier 4 through the vertical gate switch 2 and the horizontal gate switch 43, to deliver an output signal corresponding to the signal charge, from the output terminal 50. Thus, the read-out operation of one pixel is completed. As can be seen from the above explanation, the output signal obtained in the reset period and the output signal obtained at a time the signal charge is applied to the pixel amplifier, are time-sequentially delivered. By using the difference between these output signals, noise due to variations of offset of pixel amplifier and the 1/f noise of the pixel amplifier 4 can be readily suppressed.

Akimoto et al. does not disclose or suggest a reset element having both a rest transistor and a reset select transistor as presently claimed. In that connection, there is no use of reset select transistor coupled to a reset transistor to control the reset transistor. Instead, the *Akimoto et al.* reset transistor is triggered as a result of the operations of the vertical and horizontal gate switches.

As a further consequence, in *Akimoto et al.*, the horizontal scanning circuit 22 affects the horizontal gate switch transistor 43, not a reset select transistor or switch as claimed in claim 27.

Additionally, *Akimoto et al.* dose not disclose or fairly teach a select switch coupled to a vertical scanning circuit for selectively outputting the electric signal from the amplifying element. Instead, in Akimoto et al., the output of the photodiode 1 to the amplifying element 4 is gated. The amplifying element 4 output is not separately controlled.

For at least these three reasons, Akimoto et al. does not fairly anticipate the presently claimed subject matter. Applicants reserve the right to present further distinctions if and when necessary.

I. Conclusion

In view of the above amendments and remarks, Applicant submits that the claim is clearly allowable over the cited prior art, and respectfully requests early and favorable notification to that effect.

Respectfully submitted,

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By: /David R. Metzger/_
David R. Metzger
Registration No. 32,919
SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(312) 876-8000

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